

Notice of Allowability

Application No.

10/037,909

Examiner

John P Trimmings

Applicant(s)

KIM, YOUNG-WAN

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment of 9/10/2004.
2. ☒ The allowed claim(s) is/are 1-19.
3. ☒ The drawings filed on 11/09/2001 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 03112004 .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.


ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 9/10/2004.

Response to Amendment

1. The examiner acknowledges the applicant's amendment to the Specification, and approves the changes.
2. In view of the amendments to Claims 10-19, the examiner withdraws all rejections based on 35 USC 112 second paragraph.
3. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the Examiner's Amendment below.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Frank Chau, registration number 34136 on 3/8/2005.

The application has been amended wherein Claims 1 and 9 are amended as follows:

1. (Amended) An error detecting circuit comprising:

an error data storing unit for dividing a circuit implemented in a chip into predetermined areas, and outputting a plurality of error signals in response to a plurality of state error signals,

a serial chain signal,

a lock-enable signal, and

a chip error signal,

each of the plurality of state error signals being enabled when an error occurs in a corresponding predetermined area,

the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order when the error occurs in the circuit, and

the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals output from the error data storing unit,

wherein the error data storing unit stores and outputs at least one of the plurality of state error signals and,

in response to the serial chain signal, enables confirmation of at least one of the plurality of state error signals stored in the error data storing unit by observing the chip error signal.

9. (Amended) A device for detecting an error in a circuit implemented in a chip, the device comprising:

an error data storing unit for dividing the circuit into a plurality of predetermined areas and outputting a plurality of error signals in response to a plurality of state error signals,

a serial chain signal,

a lock-enable signal, and

a chip error signal,

each of the plurality of state error signals being enabled when an error occurs in a corresponding one of the plurality of predetermined areas,

the serial chain signal for reading the plurality of state error signals stored in the chip if the chip goes out of order, and

the lock-enable signal for determining whether or not to preserve the plurality of state error signals; and

an error data collecting unit for outputting the chip error signal in response to the plurality of error signals, wherein the error data storing unit stores and outputs at least one of the plurality of state error signals through the chip error signal to specifically indicate which of the predetermined areas contain the error.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance: The prior art of Gervais and Byers et al. teach an error detecting circuit having an serial chain error storage unit where failures of monitored state signals are stored, and confirmation of at least one error in the circuit is provided in response to a serial chain signal. However,

the prior arts of record taken alone, or in combination failed to teach, anticipate, suggest, or render obvious the claimed invention or the method steps of the application. Specifically, the prior arts failed to teach, anticipate, suggest, or render obvious the limitation introduced into these claims, namely: recognition of the at least one error is confirmed through the chip error signal.

Claims 2-8 and 9-19 are dependent claims upon Claims 1 and 9 respectively, and are thus also allowed in view of their dependence.


Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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